REMARKS

Favorable reconsideration of this application in view of the remarks to follow and allowance of the claims of the present application are respectfully requested.

In the present application, Claims 1-31 are pending. Of these claims, Claims 16-31 have been withdrawn from consideration, and Claims 1-15 have been rejected.

Claims 1-15 have been objected to for the alleged inconsistency in the preamble of these claims regarding "semiconducting device" and "semiconductor device" terminology. The Examiner has required applicants to select one of the two terms and make the appropriate correction.

In response, Claims 6, 8, 9, 10, and 14 have been amended to replace the term "semiconductor device" with "semiconducting device". Applicants submit that the above amendments overcome the informal objection to the claims, therefore reconsideration and withdrawal thereof is respectfully requested.

Claim 11 has been objected because the term "said dopant" allegedly lacks antecedent basis.

In response, applicants have amended Claim 11 to replace "dopant" with "doped region" and insert "doped with" prior to "an n-type dopant". Applicants submit that the above amendment to Claim 11 overcomes the objection of lacking antecedent basis, therefore reconsideration and withdrawal thereof is respectfully requested.

Claims 1, 2, 6, 9, 10, and 15 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as allegedly obvious over the disclosure of U.S. Patent 6,064,092 to Park, et al. (hereinafter "Park et al.").

More specifically, the Examiner asserts that Park et al. teach a semiconducting device comprising a channel region located in silicon 40 on insulating layer 60 of a silicon on insulating substrate including channel region 73 being thinned by presence of an underlying localized oxide region 60a on top of and in contact with buried insulating layer 60. The Examiner further alleges that the self-aligned limitation in Claim 1 and the thermal oxide or implanted oxide in Claim 9 correspond to product-by-process features.

First, applicants respectfully submit that the self-aligned limitation in Claim 1 and the thermal oxide or implanted oxide in Claim 9 are not product-by-process features. A product-by-process claim describes a product made by a specific process. However, the self-aligned limitation in Claim 1 does not describe a process of self-alignment, instead, it describes the physical structure of the semiconducting device, namely, the position of the localized oxide region in the semiconducting device. Similarly, the thermal oxide or implanted oxide in Claim 9 does not describe a process of thermal oxidation or implantation, in fact, it describes a preferred composition of the localized oxide region, namely, a thermal oxide, an implanted oxide, or a combination thereof. Thus, the self-aligned limitation in Claim 1 and the thermal oxide or implanted oxide in Claim 9 directly describe the characteristics of the claimed semiconducting device, and Claims 1 and 9 are both product claims.

Concerning the § 102 rejections, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable:

Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the claims of the present application are not anticipated by the disclosure of Park et al. since the applied reference does not teach the claimed semiconducting device recited in Claim 1. That is, Park et al. do not disclose a semiconducting device comprising a channel region located in an SOI layer of an SOI substrate, wherein said channel region is thinned by the presence of an underlying localized oxide region that is located on top of and in contact with a buried insulating layer of said SOI substrate, said localized oxide region is self-aligned to a gate region that is located above said channel region.

Park et al. disclose a semiconductor-on-insulator substrate comprising an insulating layer 60 having a surface thereon and a trench therein; a semiconductor region 73; and a mesa insulating region 60a on the bottom of the trench, wherein said semiconductor region 73 is thinned by said mesa insulating region 60a. Park et al. further teach that the mesa insulating region 60a is formed by polishing down the semiconductor substrate 40 to a semiconductor region 40' while the insulating layer 60 is bonded directly to a handling substrate 100 (See FIG. 3D, FIG. 3E, lines 53 to 67 of column 3, and lines 1-6 of column 4). Thus, the mesa insulating region 60a is not a different layer, but an integral part of the insulating layer 60. That is, the mesa insulating region 60a is merely a flat-topped elevation of the insulating layer 60. In contrast, the underlying localized oxide region 25 of the present invention is in a different layer 14, and is located on top of and in contact with the buried insulating layer 13 (See FIG. 5 and paragraph [0055]). Therefore, the semiconductor-on-insulator substrate of Park et al. is structurally different from the semiconducting device of the present invention. Since Claims 2,

6, 9, 10, and 15 are dependent on Claim 1 and include all the limitations thereof, Park et al. do not disclose the subject matter of Claims 2, 6, 9, 10, and 15 either.

In view of the above, Park et al. fail to disclose each and every element of the claims to which it is applied, therefore the § 102 rejections have been obviated.

With respect to the § 103(a) rejection, applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness as discussed below.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the cited reference must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the reference, not based on applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

First, Park et al. do not teach or remotely suggest the claimed invention. As discussed previously, the physical structure of the semiconductor-on-insulator substrate of Park et al. is markedly different from that of the semiconducting device of the present invention. Second, there is no motivation in Park et al. which suggests modifying the disclosed mesa insulating region 60a, which is part of the insulating layer 60, in such a way to arrive at the presently claimed underlying localized oxide region 25, which is in a different layer 14. In fact, the methods of forming the mesa insulating region 60a of Park et al. are drastically different from those of forming the underlying localized oxide region 25 of the present invention. While the mesa insulating region 60a is formed by polishing down the semiconductor substrate 40 to a semiconductor region 40' while the insulating layer 60 is bonded directly to a handling substrate

100 (lines 53 to 67 of column 3, and lines 1-6 of column 4), the underlying localized oxide region 25 of the present invention is formed by conducting an oxygen implantation 40 at a certain implant energy, implant dose, and dummy gate region height. Therefore, applicants respectfully submit that one skilled in the art, in view of the physical structure of the semiconductor-on-insulator substrate of Park et al. and the methods of forming the same, would not readily envision a structurally different semiconducting device that is formed through different methods, such as the semiconducting device of the present invention.

In view of the above, applicants respectfully submit that Park et al. do not render the present invention obvious. The rejections under 35 U.S.C. § 103(a) have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Further, Claims 3, 7, and 14 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Park et al. Claims 4, 5, 8, and 10-13 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Park et al. further in view of the disclosure of U.S. Patent No. 6,479,866 to Xiang (hereinafter "Xiang"). Claim 6 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Park et al. further in view of the admitted prior art.

As discussed previously, the principle reference, i.e., Park et al., spurring each of the obviousness rejections does not teach or suggest the claimed limitations of the present invention. The other applied references are further removed from the claimed invention as is evident by including those references in rejecting aspects of applicants' dependent claims. None of the other applied references teach or suggest applicants' claimed semiconducting device in which the channel region is thinned by the presence of an underlying localized oxide region that is located on top of and in contact with a buried insulating layer of said SOI substrate, said localized oxide region is self-aligned to a gate region that is located above said channel region.

Applicants therefore respectfully submit that the §103 rejections over Park et al., and further in view of other references, namely Xiang, and the admitted prior art, also fail because the above references, whether used solely or in combination, do not teach or suggest the claimed semiconducting device of the present invention.

The various §103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed semiconductor-on-insulator substrate to include applicants' claimed semiconducting device which includes, *inter alia*, an underlying localized oxide region that is located on top of and in contact with a buried insulating layer of said SOI substrate, said localized oxide region is self-aligned to a gate region that is located above said channel region. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above.

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remark, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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